Lab 5 Difference Amplifier

ECE-171L

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1. Introduction

1.1 Background Theory

Bipolar Junction Transistors (BJTs) are a type of semiconductor device that have three terminals, commonly termed as the collector, base, and emitter. BJTs come in two varieties: NPN and PNP, based on their semiconductor doping pattern. These devices are instrumental in amplifying signals, acting as switches, and in other electronic functions. The operation of a BJT is dependent on the movement of charge carriers (electrons and holes) through a semiconductor, and the transistor is "turned on" when a small input current is applied to the base, permitting a much larger current to flow from the collector to the emitter. The ratio of the output current to the input current represents the current gain, often symbolized as β.

A current mirror is a circuit designed to copy a current flowing through one active device by replicating the same current in a second active device. Widlar current mirrors, named after their provide improved performance by mitigating the Early effect, which is a variation in the current through a transistor with changes in the voltage across it. This makes the Widlar mirror superior to a basic current mirror, especially in IC designs. Current mirrors are fundamental in many analog circuits due to their ability to maintain consistent bias currents, thereby ensuring stable operation across different parts of an integrated circuit.

Differential amplifiers are also very important in analog electronics, predominantly for their ability to amplify the difference in voltages between two inputs. The primary function is to reject common signals, known as common-mode signals, on both input lines while amplifying differential signals. This capability enhances the signal-to-noise ratio and minimizes unwanted noise that might be present on both input lines. The amplification of the differential amplifier is determined by its configuration and the components used. Parameters like differential mode gain (Ad), which is the gain when the amplifier is driven by a differential input, and common mode gain (Acm), which is the gain when both inputs are driven in phase, are integral to its characterization. Another vital parameter is the Common-Mode Rejection Ratio (CMRR), which signifies the amplifier's efficiency in rejecting common-mode signals.

1.2 Experiment Purpose and Expectations

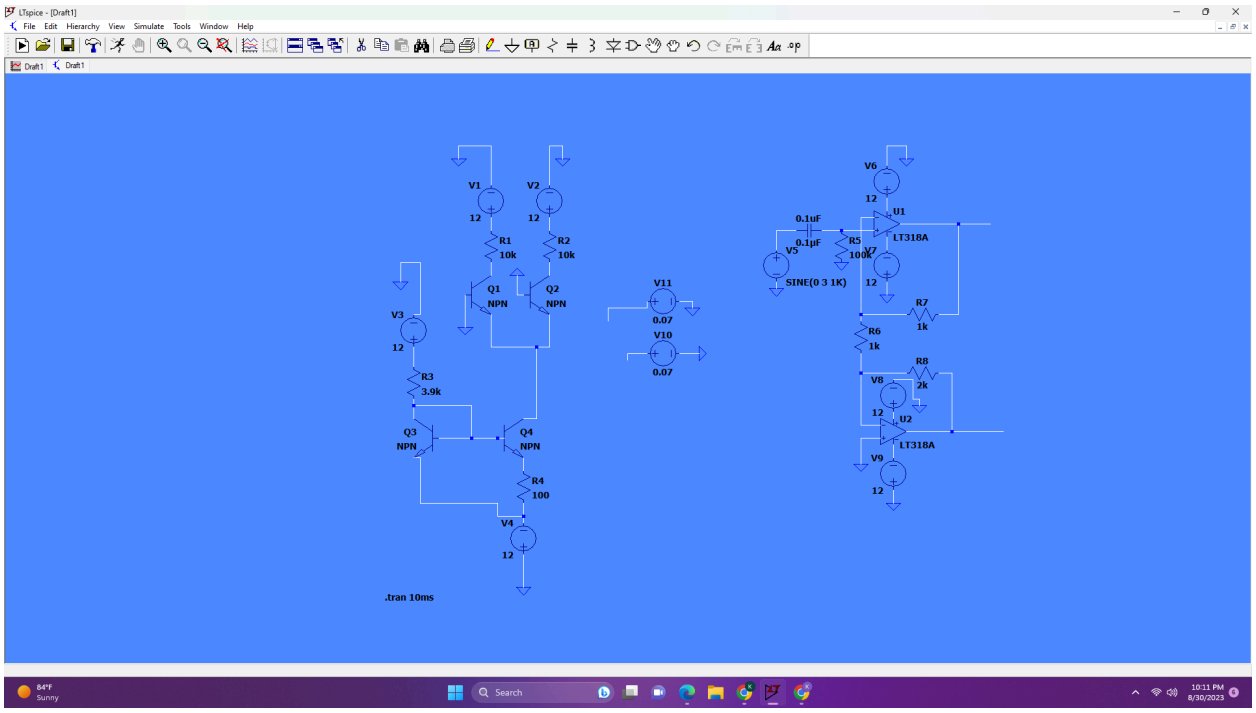
In this lab, we aim to delve into understanding the BJT differential amplifier complemented by a Widlar current mirror, an essential component in analog IC designs. By using the CA3046 NPN transistor array in an LTSpice simulation, we'll investigate both differential and common-mode

behaviors of the amplifier. This virtual approach not only emphasizes the role of the Widlar current mirror but also allows us to observe the amplifier's nuances in a controlled digital setting.

Through the LTSpice simulation, we expect to gain insights into how subtle variations in component values can dramatically alter the circuit's behavior. We'll closely study the repercussions of potential component mismatches, such as load resistors or transistors, on the output offsets.

2. Results and Analysis

2.1 Part 1



For Part one and two we will use the above circuit schematics for the differential amplifier. We are asked to find Iref, which is the current through the 3.9k ohm resistor, I0 which is the current through the collector of Q4, Ic3, and Ic4, which is the currents going through Q1 and Q2 respectively. Using the P spice simulation we found the following data. Notice the base of Q1 and Q2 are grounded.

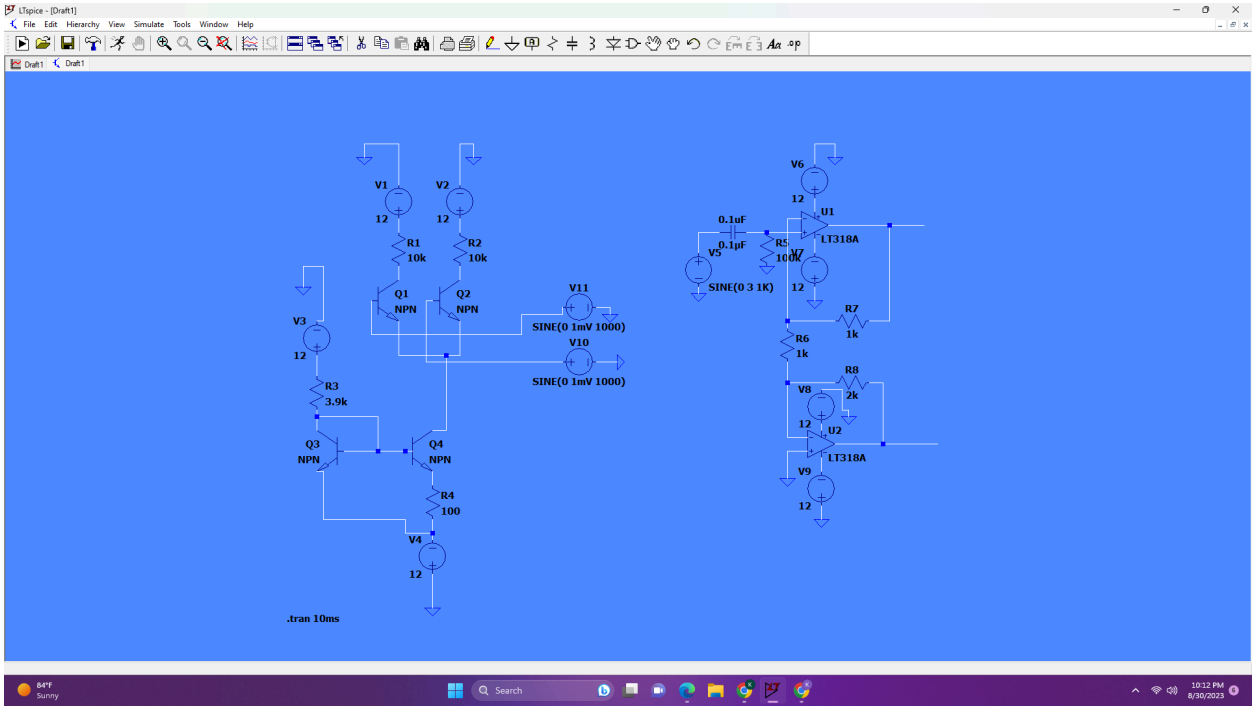
Iref mA	I0 mA	Ic3 mA	Ic4 mA
5.94357	0.589127	0.2916	0.2916

2.2 Part 2

Part 2 asks us to determine the quiescent collector voltages Vc1 and Vc2 , and DC output offset Voltage. Using LTSpice we will measure these voltages at the collectors of Q1 and Q2. The DC offset is measured as the difference between the two voltages.

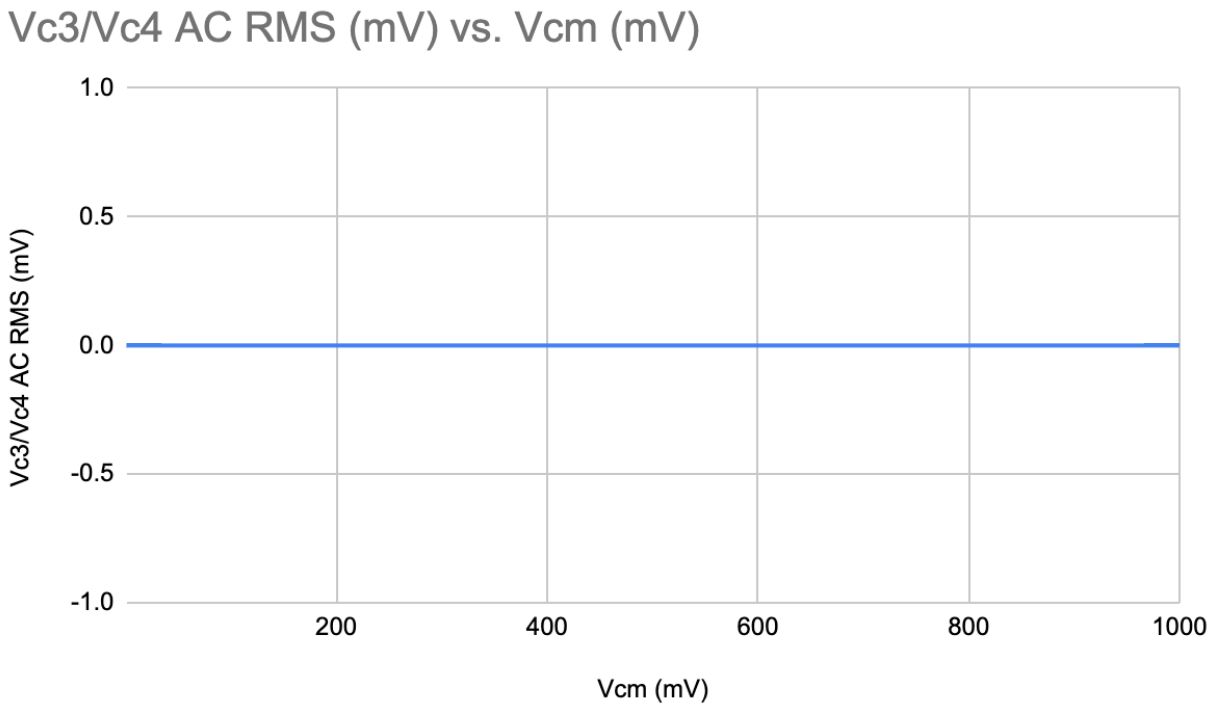
Vc1	Vc2	Offset
9.0835	9.0835	0

2.3 Part 3

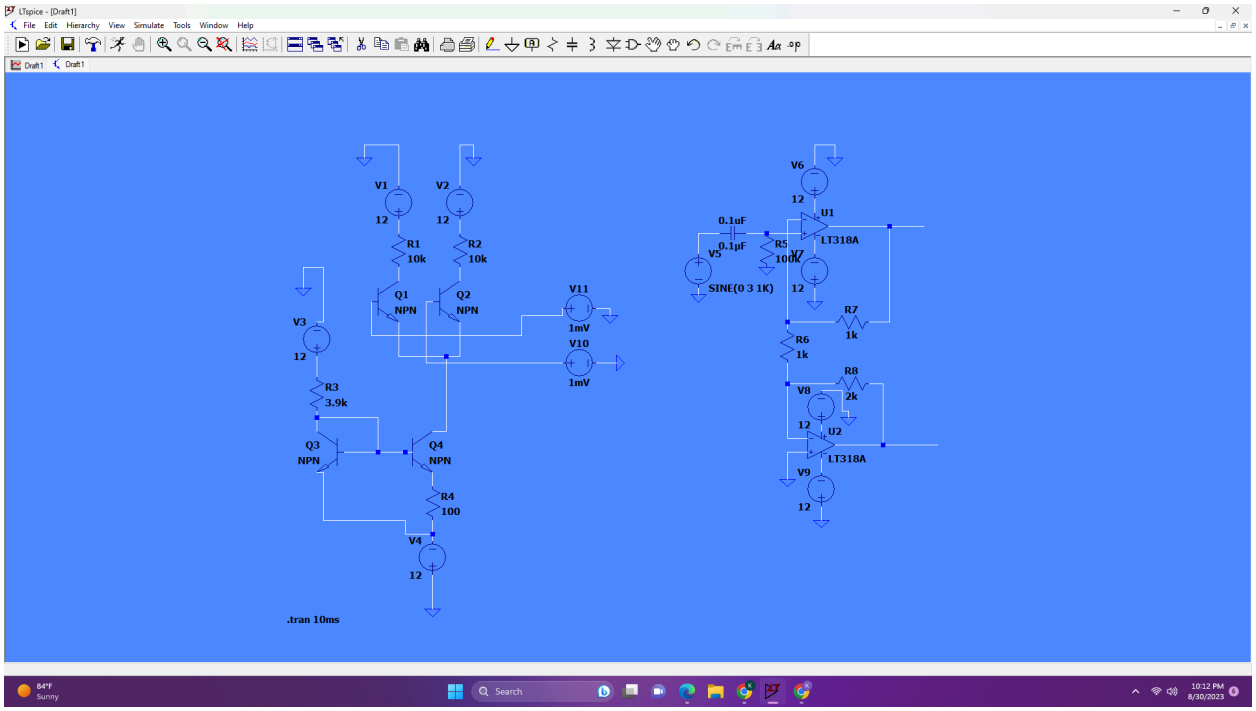


For Part three of the lab, instead of grounding the base of Q1 and Q2 we will power them with an AC sinusoidal signal in order to Measure Acm, or the common-mode gain.(shown in image above). Below is the collected Data for 10 different amplitudes of the Signal.

Vcm (mV)	ACRMS Vc3 (mV)	ACRMS Vc4
1	0	0
5	0	0
10	0	0
30	0	0
50	0	0
70	0	0
100	0	0
200	0	0
500	0	0
1000	0	0



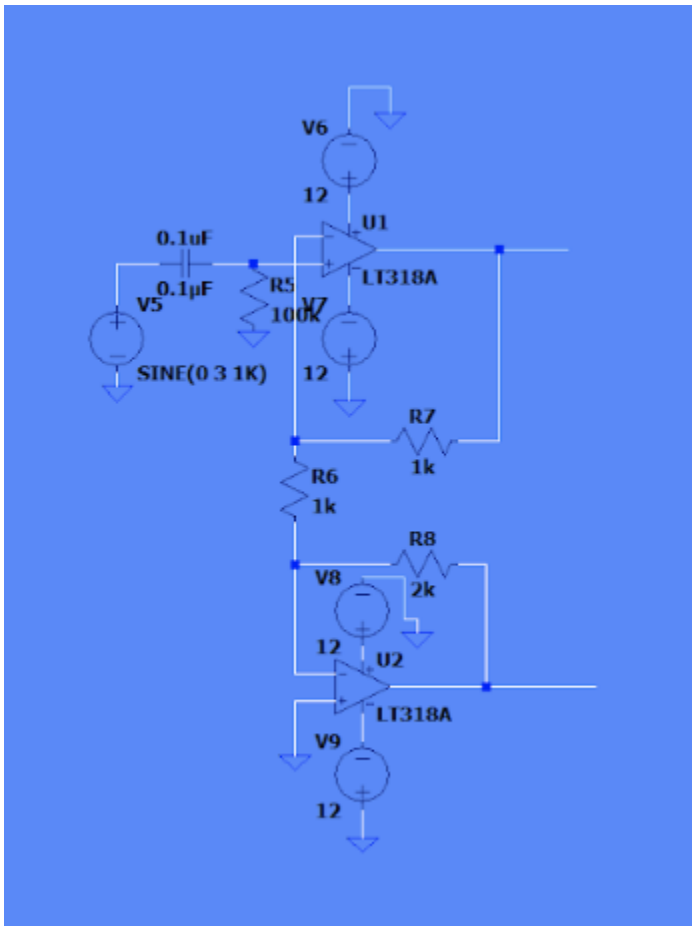
2.4 Part 4



In Part 4 of the lab we will use a DC input into the base of those transistors instead of a sinusoidal signal and observe how Vc4 ,Vbe1 ,Vbe2 , Vc1 , and Vc2 vary. We can see the schematic in the photo above.

Vcm (mV)	Vc2(mV)	Vbe3(mV)	Vbe4(mV)	Vc3(mV)	Vc4(mV)
1	-741.3604	742.36	742.36	9.08353	9.08353
5	-737.364	742.36	742.36	9.08353	9.08353
10	-732.36	742.36	742.36	9.08353	9.08353
30	-722.992	742.36	742.36	9.08353	9.08353
50	-692.36	742.36	742.36	9.08353	9.08353
70	-672.55	742.36	742.36	9.08353	9.08353
100	-659.73	742.36	742.36	9.08353	9.08353
200	-542.36	742.36	742.36	9.08353	9.08353
500	-242.36	742.36	742.36	9.08353	9.08353
1000	257.639	742.36	742.36	9.08353	9.08353

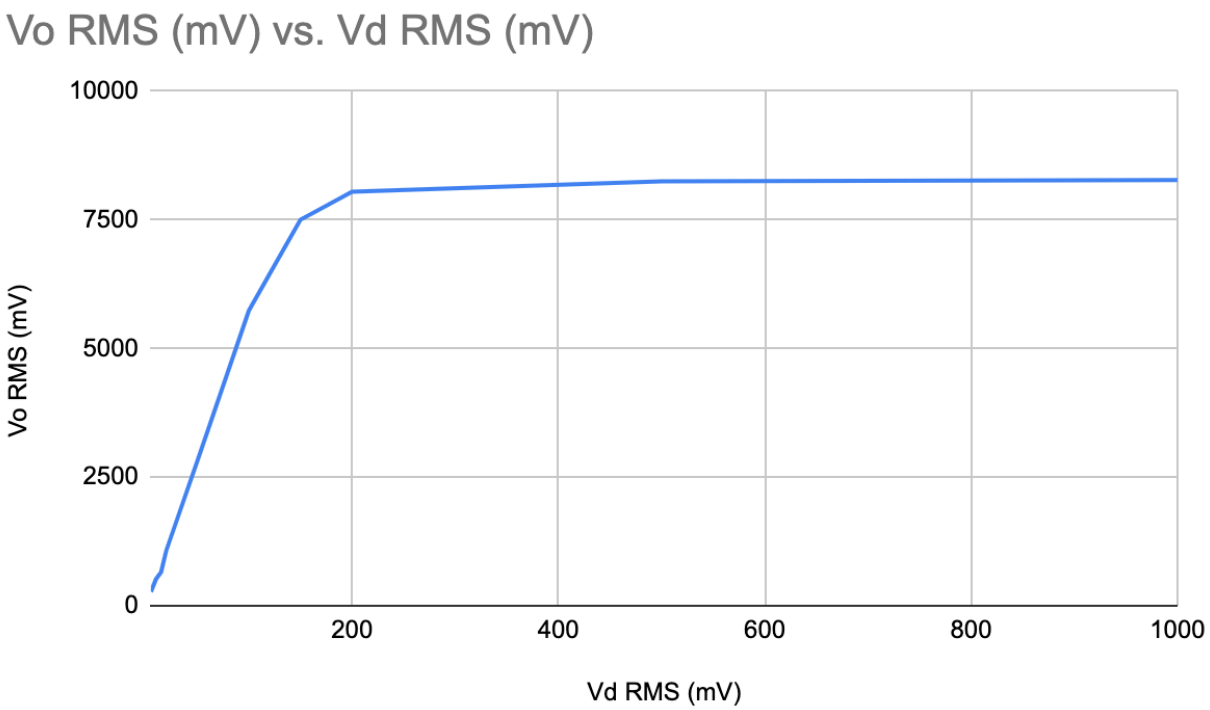
2.5 Part 5

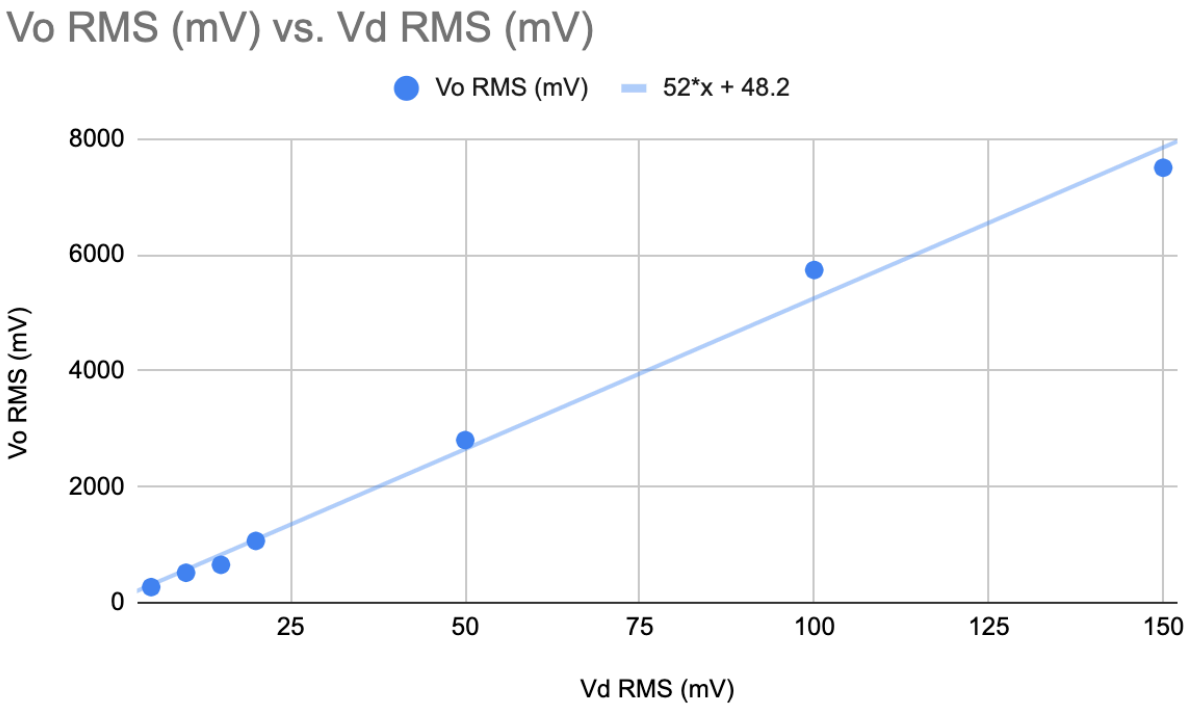


For part 5 we will use this amplifier circuit. We will measure Ad , differential-mode voltage gain, to provide a true small-signal differential input, vd , to the amplifier at vb1 and vb2. We will also determine the region of linear and non-linear amplification and produce a plot of the amplifier's transfer characteristics.

Vd RMS (mV)	Vo RMS (mV)	Gain
5	268.69	53.738
10	516.183	51.6183
15	653.36	43.557
20	1065.6	53.279
50	2804.35	56.087
100	5738.8	57.388

150	7503.038	50.02
200	8046.8	40.23
500	8251,86	16.503
1000	8273.07	8.27





In the Linear Region of operation, the Differential mode gain is around 52.

3 Conclusion

For the initial part of the lab, our primary objective was to measure Iref, I0, Ic3, and Ic4 using Ohm's Law. Following the prescribed procedure, we grounded Vbe1 and Vbe2 and took floating DC voltage measurements to derive the currents. The data shows Iref as 5.94357 mA, and a corresponding I0 of 0.589127 mA. Interestingly, the currents Ic3 and Ic4 are both equal at 0.2916 mA. This symmetry validates our measurements and implies a well-balanced differential pair.

For part 2, the observed zero offset between Vc1 and Vc2 reinforces the accuracy and precision of our simulation in LTSpice. In an ideal simulated environment, component mismatches are non-existent, which explains the perfectly balanced output.

For part three, the consistent zero output for both Vc3 and Vc4, irrespective of the varied Vcm values, underscores the ideal characteristics of the simulation. In practical scenarios, there would typically be a small, albeit discernible, common-mode gain. However, in our LTSpice simulation,

the differential amplifier perfectly rejected all common-mode signals, showcasing the model's efficacy at nullifying undesired components.

Upon analyzing the data for part 4, it's evident that as Vcm varies, the voltages Vc2, Vbe3, Vbe4, Vc3, and Vc4 remain remarkably constant. This behavior, observed within our LTSpice simulation, suggests an impressive common-mode rejection. The consistency across these voltages, even as Vcm changes, reflects the ability of our circuit to maintain stability and resist fluctuations due to common-mode signals.

For part 5, the data suggests that our differential amplifier demonstrates a clear linear amplification region when observing gains at lower values of Vd RMS. This is indicated by the relatively consistent gain values, peaking around 57.388 for an input of 100mV RMS. As the input voltage Vd RMS increases beyond this point, the gain starts to drop, suggesting the onset of non-linear amplification. Notably, at higher differential input voltages like 500mV and 1000mV RMS, the gain significantly reduces to 16.503 and 8.27 respectively, clearly indicating a non-linear behavior. Such results can be expected in real amplifiers as they approach their saturation limits.